A High-Performance Low-Power CMOS Double-Balanced IQ Down-Conversion Mixer for 2.45-GHz ISM Band Applications

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Abstract — **A 2.45GHz CMOS double-balanced IQ down-conversion switching passive mixer achieves low noise figure (NF) of 16dB, high input third-intercept point (IIP3) of -2dBm, high conversion gain (CG) of 13dB, while consuming only 4-mA from a 1.8V supply. This paper also proposes a new technique for stabilizing CG, IIP3, and NF of a CMOS passive mixer from the power supply (V_{DD}), threshold voltage (V_{TH}), and temperature variations. The proposed technique dissolves the undesired variations by providing dynamic DC biasing voltages. Measurement of various test chips shows that the CG of the mixers are all within ±0.1dB for 10% V_{DD} variations, and within ±0.75dB for temperature of –40 to 90°C.**

I. Introduction

Due to device scaling and supply voltage reduction, non-linearity of mixers is significantly affected in deep sub-micron designs. Nonetheless, high-performance low-power RF down-conversion mixer is undoubtedly desired at this era. As 3rd stage in a receiver chain (after TX-RX switch and LNA), low noise figure (NF) and high linearity of down-conversion mixer are required to minimize the degradation to overall NF and non-linearity; on the other hand, high conversion gain (CG) is required to improve signal-to-noise ratio to the following stages. Most importantly, all of the above must be achieved with low current consumption and small core die area, to have longer battery lifetime, and to reduce the cost of the fabrication, respectively. A 2.45-GHz double-balanced IQ down-conversion mixer, which is realized in 0.18µm CMOS technology, is presented in this paper, which achieves: low NF of 16dB, high IIP3 of -1dBm, high CG of 13dB, low current consumption of 4-mA at a single 1.8V power supply, and small core die area (without pads) of 0.67mm^2.

CMOS passive mixer is becoming more favorable [1] – [4] as its linearity performance is not affected by the low supply voltage (V_{DD}). Various reports had shown excellent IP3 results and acceptable noise figure from CMOS passive mixers. However, one of the major problems of the topology is that the CG, linearity performance, and NF is strongly dependent of the V_{DD}, process, and temperature variations. As the V_{TH} of sub-micron transistors can vary as much as ±10% at different process corner, the transceiver's sensitivity will be affected undesirably from chip to chip, and thus worsening the CMOS production yields. This paper introduces a new dynamic DC compensation technique to overcome the V_{TH}, V_{DD}, and temperature variations of the CMOS passive mixer, enabling the topology out-performs CMOS Gilbert Cell active mixer. Measurement of various test chips shows that the CG of the mixers are all within ±0.1dB for 10% V_{DD} variations, and within ±0.75 for temperature of –40 to 90°C, by using the proposed technique.

II. CIRCUIT DESCRIPTION

A. Block Diagram

Fig. 1 shows the block diagram of the double-balanced IQ down-conversion mixer design. It consists of a differential RF matching network (MN), a LO polyphase filter (PF), in-phase (I) and quadrature (Q) mixer cores (MIXs), LO Amplifiers (LOAs), and IF Amplifiers (IFAs). The RF down-conversion mixer presented in this paper is to be used in a low-IF (1-MHz) receiver architecture. In such architecture, the mixer is preceded with TX-RX switch and LNA, and is followed by IF complex filter. Therefore, the input of the mixer is required to conjugate match to the output impedance of the LNA, and the IF outputs are to drive high impedance.

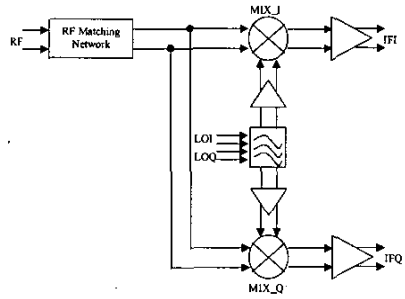

Fig. 1. Block diagram of the double balanced IQ down-conversion mixer design.

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B. Mixer Core

Active mixers that based on Gilbert Cell topology are generally able to provide higher CG. However, in deep sub-micron designs, this topology has difficulty in providing high CG and high linearity in the same time, due to the voltage headroom limitation. Hence a switching passive mixer, in which linearity is independent of the voltage headroom, has been selected as the core of the down-conversion mixer. Although there are several other topologies show better linearity performance as in [1] and [2], those topologies often exhibit undesirably high noise figure.

Fig. 2 shows the schematic diagram for the differential passive mixer core [3], [4]. With this topology, the transistors in passive mixer core do not draw any DC current. During its operation, a pair of transistors in passive mixer core is switched on while the other is switched off simultaneously. In the switching process, the transistors' on-resistance plays an important role on contributing to the NF. Consequently, increasing aspect ratio of the transistors could help in better noise performance. In contrast, small transistor sizes are desirable because it introduces only small capacitance to LOAs, thus reducing required current consumption. Besides, small aspect ratio and zero drain-source voltage of transistors in passive mixer core can improve LO-to-RF isolation. To minimize the occupied die area, the DC bias voltage at RF ports is passed over to the input differential pairs of the IF amplifiers.

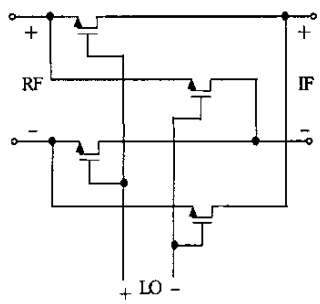


Fig. 2. Schematic Diagram of Differential Passive Mixer Core.

C. LO Polyphase Filter (PF)

Phase error between I and Q IF ports will affect image rejection at following stage, i.e. complex filter. Therefore, a three-stage LO PF [1] is incorporated into the mixer design to ensure quadrature LO signals are feeding into the LOAs. The three-stage LO PF is centered at 2.4-, 2.45-, and 2.5-GHz to ensure accurate phase control at the desired band. A major drawback of using a three-stage PF is that it attenuates the LO signals by at least 3 dB.

D. LO Amplifier (LOA)

As double-balanced mixer are more susceptible to noise in the LO signals [5], LOA can make use of resistors to achieve desired voltage swings at the LO ports of mixer core. Fig. 4 shows the schematic diagram of the LOA. The LOA employs a special technique – capacitive source-coupling [6] – to ensure the DC voltages of the output of each stage are insensitive to short-channel transistors mismatch. This technique avoids the use of DC blocking capacitors at the outputs of each stage. Hence, silicon area and the extra current consumption to drive bottom plates of capacitors can be saved.

One of the important considerations on the LOA design is to make mixer CG independent of the LOA output power. Due to the fact that VCO output power varies with process by nature, this technique allows better control in gain and sensitivity spread of the receiver, hence the process yields. Therefore, the input power compression point of LOA is designed to happen before the desired input power, thereby saturates the output swings. In this design, the LOA is designed to amplify –10 dBm LO input to 1-V peak-to-peak voltage swings.

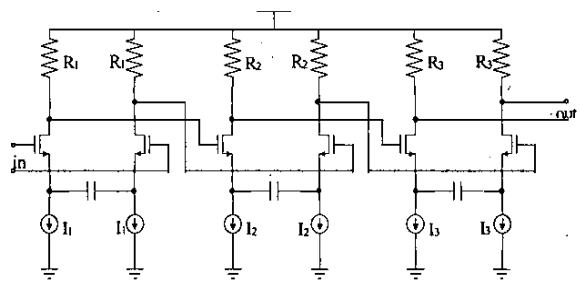


Fig.3. Schematic Diagram of LOA.

E. Dynamic DC Bias Circuit (DBC)

A hypothesis is drawn: maximum stability of the conversion gain of a mixer can be achieved by simply maintain the V_{EFF} ($=V_{GS}-V_{TH}$) of the frequency conversion transistors in all conditions. Thus, the passive mixer design employs a dynamic DC bias circuit to maintain V_{EFF} of transistors in mixer core to be constant from temperature of –40 to 90°C, and ±10% V_{TH} and V_{DD} variations.

Fig. 5 shows the dynamic DC bias circuit (DBC). In Fig. 5, V_{BG} is the bandgap voltage (i.e. approximately 1.18V) and V_X is to bias both the RF ports of passive mixer core. Both R_{REF} and I_B ensure a set DC value at the 3rd stage of LOAs. M_{MX}, which is having same size and layout pattern as transistors in mixer core, performs

process tracking. Therefore, if the V_{TH} of the process decreases, V_X will decrease accordingly by same amount as the DC current derived from bandgap voltage remain unchanged, ensuring V_{EFF} of passive mixer core remains constant. Likewise, both temperature and V_{DD} variations are tracked as the DBC provides a dynamically tracking biasing voltage to maintain the V_{EFF} of passive mixer core. Due to near-zero DC current flows through passive mixer core, R_A is to introduce another constant voltage-drop and to minimize DC current flows through transistor M_{MX}.

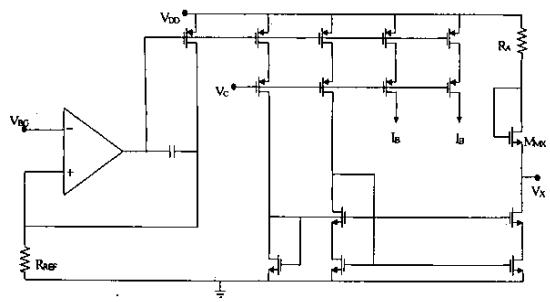


Fig. 5. Dynamic DC Bias Circuit to Compensate V_{TH}, V_{DD}, and Temperature Effects.

III. EXPERIMENTAL RESULTS

Fig. 6 shows a microphotograph of the double-balanced IQ down-conversion mixer test chip. The differential RF inputs are fed into the test chip from two middle pads on the left; on the other hand, the differential and quadrature LO inputs are fed into the test chip from four middle pads on the right. Middle pads are used in both cases to minimize the differences in bond wire length that may introduce phase and amplitude errors. The remaining LO phase and amplitude errors are corrected by the on-chip LO PF. I and Q IF outputs, V_{DD}, and ground that required less care are fed into the test chip through the rest of the pads.

The layout is very symmetrical to obtain good common-mode cancellations. To avoid LO-to-RF feedthrough, the I and Q LOAs are surrounded with ground plane (ptap connected to ground) to improve isolation. In addition, I and Q passive mixer cores are "well-protected" by ptap connected to ground and ntap connected to V_{DD} to minimize noise injection into the cores. Empty spaces are filled with MOS capacitors for supply de-coupling. Due to transistor sizes in the mixer cores are extremely small and sensitive to ESD, in-house RF ESD pads that reveal 50-fF of capacitance each, are used for test purposes. The area of the down-conversion mixer circuit is 0.67 mm^2 (without pads).

The test chips are packaged in a 24 Lead Glass Flatpack Gullwing package, and mounted on a FR-4 material PCB. Several components are used to ensure accurate measurements, including: (1) MCLI 180° and 90° power splitters (HJ-6 and HB-3) to generate differential and quadrature signals on both LO and RF ports; (2) Maxim unity gain buffers, MAX496, on each IF outputs to drive 50Ω; (3) Mini-Circuits ZFSCJ-2-2 IF combiners to combine differential signals; (4) Mini-Circuits ZFL-1000LN Preamp for noise calibration purposes. Both the CG and NF measurements utilize Rohde & Schwarz SMIQ06B Spectrum Analyzer. All the losses in power splitters, buffers, and IF combiners are fully calibrated. Besides, additional 1dB losses on bond wires, package leads, and PCB traces at the RF inputs are also compensated. All the measurements are also repeated in temperature chamber at –40 to 90°C.

The measured performance of the mixer test chip is summarized in Table I. Fig. 7A shows the CG of a sample versus V_{DD} and temperature, and Fig. 7B shows the CG of different samples versus V_{DD} at room temperature (25°C). The measurement results shows that the CG of various samples are all within ±0.1dB for 10% V_{DD} variations, and all are within ±0.75dB for temperature of –40 to 90°C, proving the validity of the hypothesis that maximum stability can be achieved through maintaining V_{EFF} of the frequency conversion transistors. Fig. 8 shows the measured input IP3 of the mixer design at 25°C and 1.8V supply, achieving IIP3 of –1dBm.

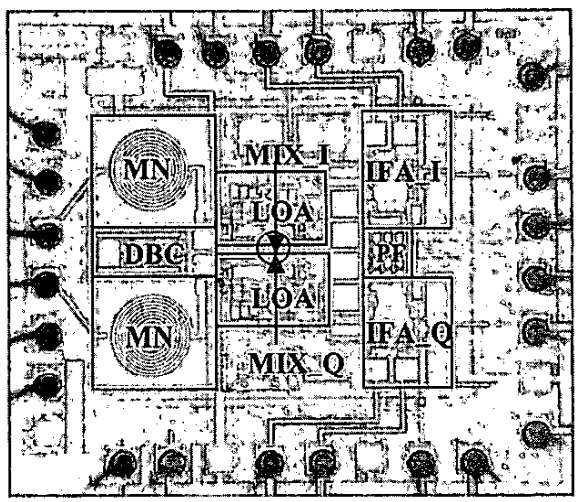
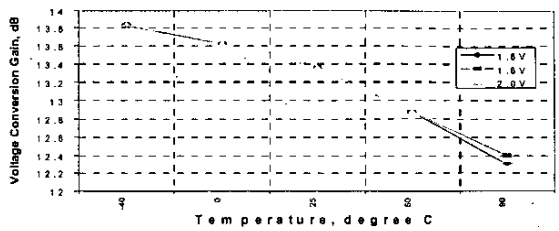


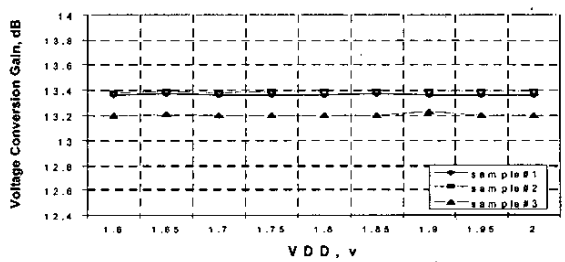
Fig. 6. Microphotograph of the 2.45GHz CMOS Double-Balanced IQ Down-Conversion Mixer.

Table I.
Summary of Measured Performance of Double-Balanced IQ Down-Conversion Mixer test chip

Technology	CMOS 0.18 μm 1poly 6 metals		
Temperature, °C	-40	25	90
f_{RF}, GHz	2.45	2.45	2.45
f_{LO}, GHz	2.449	2.449	2.449
f_{IF}, MHz	1	1	1
V_{DD}, V	1.8	1.8	1.8
Current, mA	4.13	4.02	3.91
LO Power, dBm	-10	-10	-10
CG, dB	13.82	13.36	12.4
Gain Flatness, dB (of ±2dB LO Power)	±0.3	±0.3	±0.3
P1dB, dBm	-12	-12	-12
IIP3, dBm	-1	-1	-1
SSB NF, dB	15	16	18
LO-RF Isolation, dBc	30	30	30



(A)



(B)

Fig. 7 (A) CG Vs. Temperature and V_{DD} of a Sample (B) CG Vs. V_{DD} for Different Samples at 25 °C.

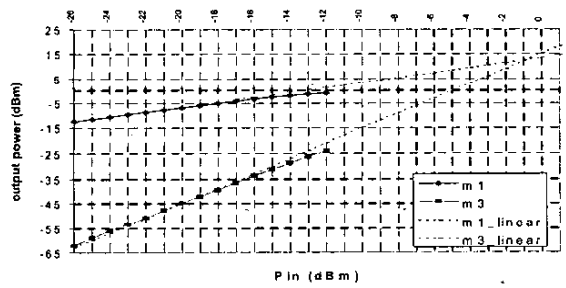


Fig. 8 Measured Input IP3 at 1.8V and 25°C.

IV. CONCLUSION

In this paper a high-performance low-power CMOS IQ down-conversion mixer has been presented. It employs switching passive mixer core as mixing device to achieve low noise figure and high linearity, and its small transistor sizes also relax the current consumption at LOAs. Special technique – capacitive source degeneration – is also used to achieve low current consumption in LOAs. In addition, the voltage conversion gain of the mixer circuit is saturation (within ±0.3dB) for ±2dB about nominal LO input power. Thus, the receiver gain and sensitivity are independent of the VCO power variations.

Test chips are realized in a standard 0.18-μm CMOS technology. The achieved SSB noise figure, IIP3, LO-to-RF isolation are 13dB, -1dBm, and 30dB, respectively, and can achieve most receiver system specifications. Most importantly, these performances are achieved with only 4-mA at 1.8V supply, occupied only 0.67mm^2 core die area, and designed to improve production yields, making the mixer design really attractive to industries.

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REFERENCES

[1] Jan Crols and Michiel Steyaert, CMOS Wireless Transceiver Design, Kluwer Academic Publishers, pp. 139-150, 1997.

[2] M.S.J. Steyaert, Bram Demuer, Paul Leroux, Marc Borremans, "Low-Voltage Low Power CMOS-RF Transceiver Design," IEEE Transactions on Microwave Theory and Techniques, vol. 50, No. 1, pp. 281 – 287, Jan. 2002.

[3] Thomas H. Lee, The Design of CMOS Radio Frequency Integrated Circuits, Cambridge, pp. 331-335, 1998.

[4] A. R. Shahani, D. K. Shaeffer, and T.H. Lee, "A 12-mW Wide Dynamic Range CMOS Front-End for a Portable GPS Receiver," IEEE J. Solid-State Circuit, vol. 32, pp.2061 – 2070, Dec. 1999.

[5] Behzad Razavi, RF Microelectronics, Prentice Hall PTR, pp. 180-200, 2000.

[6] U. Dasgupta, W.G. Yeoh, C.G. Tan, S.J. Wong, H. Mori, R. Singh, and M. Itoh, "A Transmit/Receive IF Chip-Set for WCDMA Mobiles in 0.35-μm CMOS," 2002 IEEE Transactions on Microwave Theory and Techniques, pp. 2443-2452, Nov. 2000.